	Application No.	Applicant(s)
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Notice of Allowability	10/603,616	IWAMI ET AL.
Notice of Anowability	Examiner	Art Unit
	VIJAY SHANKAR	2673
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. X This communication is responsive to 6-26-2003.		
2. The allowed claim(s) is/are <u>1-10</u> .		
3. The drawings filed on 10-23-2003 are accepted by the Examiner.		
 4.		
3. Copies of the certified copies of the priority documents have been received in this national stage application from the		
International Bureau (PCT Rule 17.2(a)).		
* Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		
5. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.		
6. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.		
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached		
1) hereto or 2) to Paper No./Mail Date		
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date		
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).		
7. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.		
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Attachment(s) 1. ☑ Notice of References Cited (DTO 802)	E Nation of Information	otent Application (PTO 152)
 Notice of References Cited (PTO-892) Dotice of Draftperson's Patent Drawing Review (PTO-948) 	6. ☐ Interview Summary	atent Application (PTO-152)
Information Disclosure Statements (PTO-1449 or PTO/SB/0.	Paper No./Mail Date	e
Paper No./Mail Date		
 Examiner's Comment Regarding Requirement for Deposit of Biological Material 	8. ☑ Examiner's Stateme 9. ☐ Other	nt of Reasons for Allowance
		VIJAY SHANKAR Primary Examiner Art Unit: 2673

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DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The corrected drawings Figure.6 were received on 10-23-2003. These drawings are acceptable and approved by the Examiner.

Allowable Subject Matter

3. Claims 1-10 are allowed.

The following is an examiner's statement of reasons for allowance: The prior arts

Nagaoka (US 2003/0184537A1), Noborio (6,072,447), Ide et al (6,304,038), Ide

(6,333,738), Berkey et al (6,337,763) fails to disclose or recite a display panel driver for

driving a display panel in which capacitive light emitting cells serving as pixels are

formed at intersections between a plurality of row electrodes serving as display lines

and a plurality of column electrodes intersecting with the row electrodes in accordance

with pixel data for the pixels based on an input video signal, the display panel driver

comprising: a pixel data pulse generation circuit which generates pixel data pulses by

connecting the column electrodes and a power source line in accordance with the pixel

data to apply the pixel data pulses to the column electrodes; a resonance pulse power

circuit which generates a resonance pulse power source voltage to apply the resonance

pulse power source voltage to the power source line, the resonance pulse power circuit

changing the resonance amplitude of the resonance pulse power source voltage while

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keeping a maximum voltage of the resonance pulse power source voltage in accordance with a pattern of a pulse sequence of the pixel data pulses; a power prediction circuit which determines a predicted power consumption of the resonance pulse power circuit based on the pixel data for one field; and a power consumption control circuit which controls the pixel data pulse generation circuit so as to adjust the power consumption of the resonance pulse power circuit in accordance with the predicted power consumption; wherein the pixel data pulse generation circuit is divided into a plurality of IC chips respectively corresponding to column electrode groups that are made of a predetermined number of column electrodes; and wherein the IC chips are mounted on a plurality of flexible wiring boards that are respectively connected to the power source line and the column electrodes in the resonance pulse power circuit formed on the substrate of the display panel as claimed in Claim 10.

The closest prior art, Nagaoka (US 2003/0184537A1), Noborio (6,072,447), Ide et al (6,304,038), Ide (6,333,738), Berkey et al (6,337,763), either singularly or in combination, fail to anticipate or render the above underlined limitations obvious.

Also, the prior arts Nagaoka (US 2003/0184537A1), Noborio (6,072,447), Ide et al (6,304,038), Ide (6,333,738), Berkey et al (6,337,763) fails to disclose or recite a display panel driver for driving a display panel in which capacitive light emitting cells serving as pixels are formed at intersections between a plurality of row electrodes serving as display lines and a plurality of column electrodes intersecting with the row

electrodes in accordance with pixel data for the pixels based on an input video signal, the display panel driver comprising: a pixel data pulse generation circuit which generates pixel data pulses by connecting the column electrodes and a power source line in accordance with the pixel data to apply the pixel data pulses to the column electrodes; a resonance pulse power circuit which generates a resonance pulse power source voltage to apply the resonance pulse power source voltage to the power source line, the resonance pulse power circuit changing the resonance amplitude of the resonance pulse power source voltage while keeping a maximum voltage of the resonance pulse power source voltage in accordance with a pattern of a pulse sequence of the pixel data pulses; a power prediction circuit which determines a predicted power consumption of the resonance pulse power circuit based on the pixel data for one field; and a power consumption control circuit which controls the pixel data pulse generation circuit so as to adjust the power consumption of the resonance pulse power circuit in accordance with the predicted power consumption as claimed in Claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Appl. No. 10/603,616
Docket No. Q76222
Preliminary Amdt. Dated October 23, 2003
Annotated marked-up Drawings



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FIG. 6

